



8355/8355-2 16,384-BIT ROM WITH I/O

- 2048 Words × 8 Bits
- Single +5V Power Supply
- Directly Compatible with 8085A and iAPX 88 Microprocessors
- 2 General Purpose 8-Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- Internal Address Latch
- 40-Pin DIP

The Intel® 8355 is a ROM and I/O chip to be used in the 8085A and iAPX 88 microprocessor systems. The ROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 450 ns to permit use with no wait states in the 8085A CPU.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 lines and each I/O port line is individually programmable as input or output.

The 8355-2 has a 300 ns access time for compatibility with the 8085A-2 and 5 MHz iAPX 88 microprocessors.

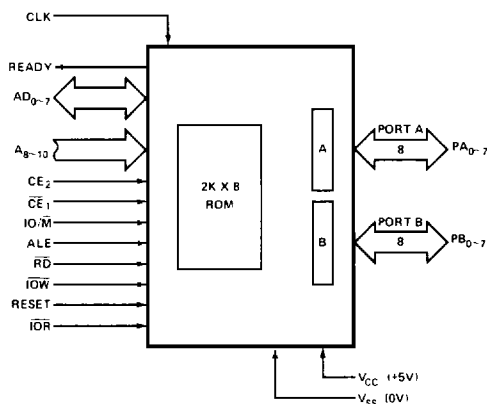
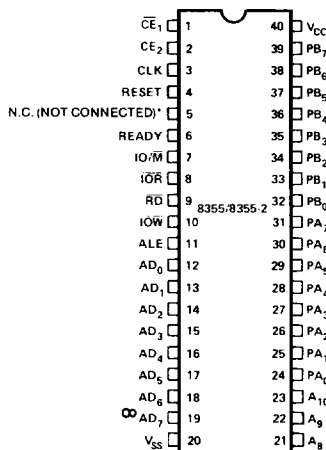


Figure 1. Block Diagram



* For 8755A compatibility, pin 5 should be directly tied to VCC.

Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
ALE	I	Address Latch Enable: When high, AD ₀₋₇ , IO/M, A ₈₋₁₀ , CE ₂ , and CE ₁ enter the address latches. The signals (AD, I/O/M, A ₈₋₁₀ , CE ₂ , CE ₁) are latched in at the trailing edge of ALE.
AD ₀₋₇	I	Address/Data Bus (Bidirectional): The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B is selected based on the latched value of AD ₀ . If RD or IOR is low when the latched chip enables are active, the output buffers present data on the bus.
A ₈₋₁₀	I	Address Bus: High order bits of the ROM address. They do not affect I/O operations.
CE ₁ CE ₂	I	Chip Enable Inputs: CE ₁ is active low and CE ₂ is active high. The 8355 can be accessed only when BOTH Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD ₀₋₇ and READY outputs will be in a high impedance state.
IO/M	I	I/O Memory: If the latched IO/M is high when RD is low, the output data comes from an I/O port. If it is low, the output data comes from the ROM.
RD	I	Read: If the latched Chip Enables are active when RD goes low, the AD ₀₋₇ output buffers are enabled and output either the selected ROM location or I/O port. When both RD and IOR are high, the AD ₀₋₇ output buffers are 3-stated.
IOW	I	I/O Write: If the latched Chip Enables are active, a low on IOW causes the output port pointed to by the latched value of AD ₀ to be written with the data on AD ₀₋₇ . The state of IO/M is ignored.
CLK	I	Clock: Used to force the READY into its high impedance state after it has been forced low by CE ₁ low, CE ₂ high and ALE high.
READY	O	READY: A 3-state output controlled by CE ₁ , CE ₂ , ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK.
PA ₀₋₇	I/O	Port A: General purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and IOW is low and a 0 was previously latched from AD ₀ , AD ₁ . Read operation is selected by either IOR low and active Chip Enables and AD ₀ and AD ₁ low, or IO/M high, RD low, active chip enables, and AD ₀ and AD ₁ , LOW.
PB ₀₋₇	I/O	Port B: This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD ₀ and a 0 from AD ₁ .
RESET	I	Reset: An input high causes all pins in Port A and B to assume input mode. (Clear DER Register).
IOR	I	I/O Read: When the Chip Enables are active, a low on IOR will output the selected I/O port onto the AD bus. IOR low performs the same function as the combination IO/M high and RD low. When IOR is not used in a system, IOR should be tied to V _{CC} ("1").
V _{CC}		Voltage: +5 volt supply.
V _{SS}		Ground: Ground Reference.

FUNCTIONAL DESCRIPTION

ROM Section

The 8355 contains an 8-bit address latch which allows it to interface directly to MCS-48, MCS-85, and iAPX 88/10 Microcomputers without additional hardware.

The ROM section of the chip is addressed by an 11-bit address and the Chip Enables. The address and levels on the Chip Enable pins are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and $\overline{IO/\overline{M}}$ is low when \overline{RD} goes low, the contents of the ROM location addressed by the latched address are put out through AD_{0-7} output buffers.

I/O Section

The I/O section of the chip is addressed by the latched value of AD_{0-1} . Two 8-bit Data Direction Registers (DDR) in 8355 determine the input/output status of each pin in the corresponding ports. A "0" in a particular bit position of a DDR signifies that the corresponding I/O port bit is in the input mode. A "1" in a particular bit position signifies that the corresponding I/O port bit is in the output mode. In this manner the I/O ports of the 8355 are bit-by-bit programmable as inputs or outputs. The table summarizes port and DDR designation. DDR's cannot be read.

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IO/\overline{M}}$ goes low and the Chip Enables are active, the data on the AD_{0-7} is written into I/O port selected by the latched value of AD_{0-1} . During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of $\overline{IO/\overline{M}}$. The actual output level does not change until $\overline{IO/\overline{M}}$ returns high (glitch free output).

A port can be read out when the latched Chip Enables are active and either \overline{RD} goes low with $\overline{IO/\overline{M}}$ high, or \overline{IOR} goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7} .

To clarify the function of the I/O ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.

Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the output latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

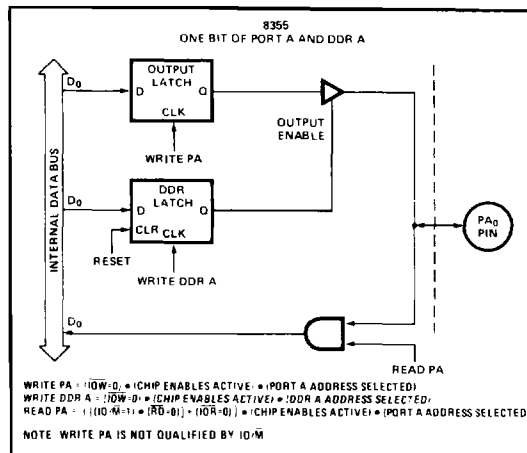


Figure 3. 8355 One Bit of Port A and DDR A

SYSTEM APPLICATIONS

System Interface with 8085A and iAPX 88

A system using the 8355 can use either one of the two I/O Interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both \overline{CE}_2 and \overline{CE}_1 . By using a combination of unused address lines A_{11-15} and the Chip Enable inputs, the system can use up to 5 each 8355's without requiring a CE decoder. See Figure 5a and 5b.

If a memory mapped I/O approach is used the 8355 will be selected by the combination of both the Chip Enables and $\overline{IO/\overline{M}}$ using AD_{8-15} address lines. See Figure 4.

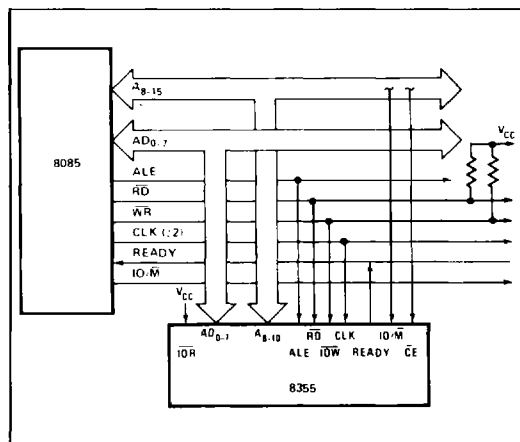


Figure 4. 8355 in 8085A System (Memory-Mapped I/O)

IAPX 88 FIVE CHIP SYSTEM:

- 1.25 K Bytes RAM
- 2 K Bytes ROM
- 38 I/O Pins
- 1 Internal Timer
- 2 Interrupt Levels

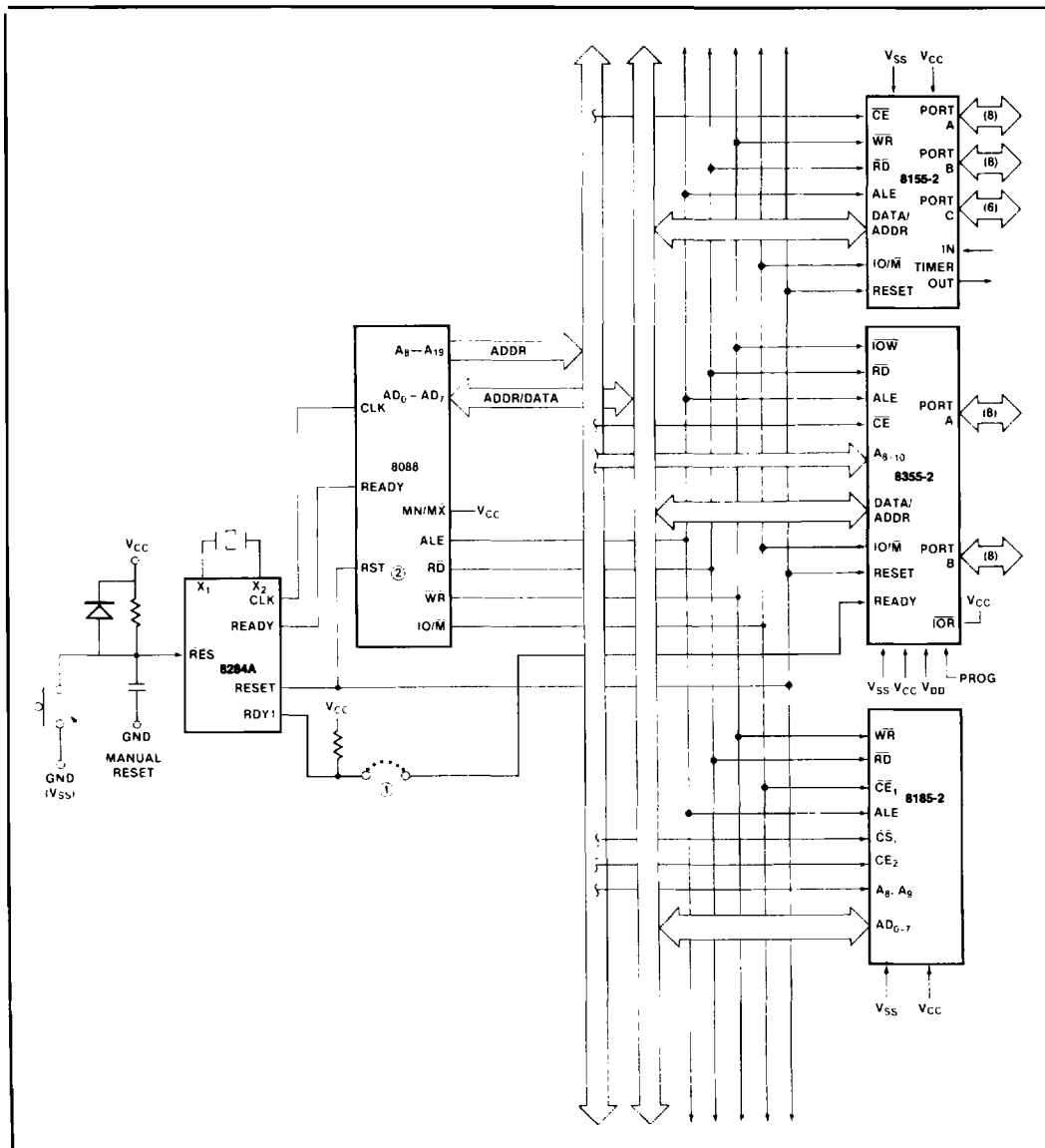


Figure 5a. IAPX 88 Five Chip System Configuration

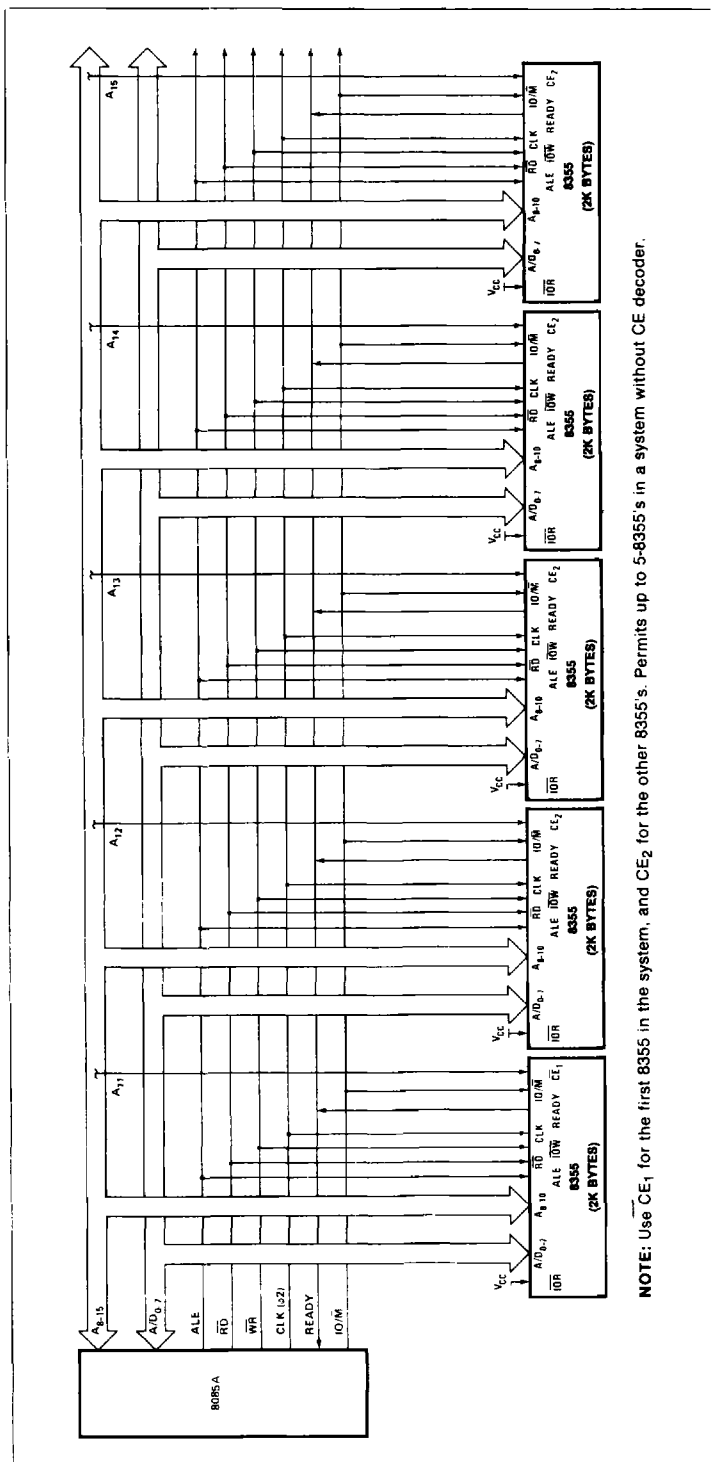


Figure 5b. 8355 in 8085A System (Standard I/O)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to -70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	
With Respect to Ground	-0.5V to +7V
Power Dissipation	1.5W

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V _{IL}	Input Low Voltage	-0.5	0.8	V	V _{CC} = 5.0V
V _{IH}	Input High Voltage	2.0	V _{CC} +0.5	V	V _{CC} = 5.0V
V _{OL}	Output Low Voltage		0.45	V	I _{OL} = 2mA
V _{OH}	Output High Voltage	2.4		V	I _{OH} = -400μA
I _{IL}	Input Leakage		10	μA	0V ≤ V _{IN} ≤ V _{CC}
I _{LO}	Output Leakage Current		±10	μA	0.45V ≤ V _{OUT} ≤ V _{CC}
I _{CC}	V _{CC} Supply Current		180	mA	

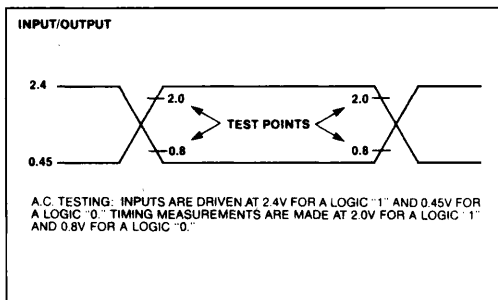
A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

Symbol	Parameter	8355		8355-2		Units
		Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	320		200		ns
T ₁	CLK Pulse Width	80		40		ns
T ₂	CLK Pulse Width	120		70		ns
t _r , t _f	CLK Rise and Fall Time		30		30	ns
t _{AL}	Address to Latch Set Up Time	50		30		ns
t _{LA}	Address Hold Time after Latch	80		45		ns
t _{LC}	Latch to READ/WRITE Control	100		40		ns
t _{RD}	Valid Data Out Delay from READ Control*		170		140	ns
t _{AD}	Address Stable to Data Out Valid**		450		300	ns
t _{LL}	Latch Enable Width	100		70		ns
t _{RDF}	Data Bus Float after READ	0	100	0	85	ns
t _{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t _{CC}	READ/WRITE Control Width	250		200		ns
t _{DW}	Data In to Write Set Up Time	150		150		ns
t _{WD}	Data In Hold Time After WRITE	30		10		ns
t _{WP}	WRITE to Port Output		400		300	ns
t _{PR}	Port Input Set Up Time	50		50		ns
t _{RP}	Port Input Hold Time	50		50		ns
t _{RYH}	READY HOLD Time	0	160	0	160	ns
t _{ARY}	ADDRESS / CE ₁ to READY		160		160	ns
t _{RV}	Recovery Time Between Controls	300		200		ns
t _{RDE}	READ Control to Data Bus Enable	10		10		ns

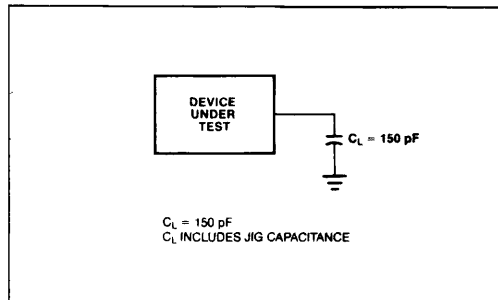
*Or T_{AD}-(T_{AL} + T_{LC}), whichever is greater.

**Defines ALE to Data out Valid in conjunction with T_{AL}.

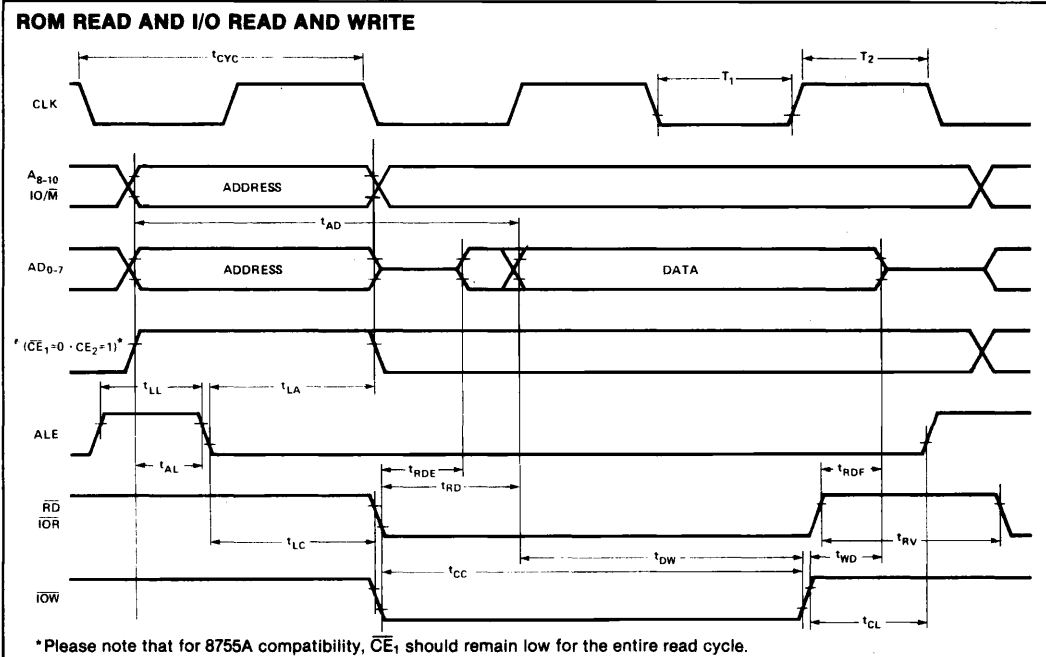
A.C. TESTING INPUT, OUTPUT WAVEFORM



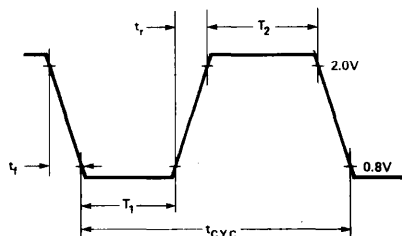
A.C. TESTING LOAD CIRCUIT



WAVEFORMS



8355 CLOCK SPECIFICATIONS



WAVEFORMS (Continued)

