8218/8219
BIPOLAR MICROCOMPUTER BUS CONTROLLERS FOR MCS-80® AND MCS-85® FAMILIES

- **8218 for Use in MCS-80® Systems**
- **8219 for Use inMCS-85® Systems**
- **Coordinates the Sharing of a Common Bus Between Several CPU's**
- **Reduces Component Count in Multimaster Bus Arbitration Logic**
- **Single +5 Volt Power Supply**
- **28 Pin Package**

The 8218 and 8219 Microcomputer Bus Controllers consist of control logic which allows a bus master device such as a CPU or DMA channel to interface with other masters on a common bus, sharing memory and I/O devices. The 8218 and 8219 consist of:

1. Bus Arbitration Logic which operates from the Bus Clock ($\overline{BCLK}$) and resolves bus contention between devices sharing a common bus.
2. Timing Logic which when initiated by the bus arbitration logic generates timing signals for the memory and I/O command lines to guarantee set-up and hold times of the address/data lines onto the bus. The timing logic also signals to the bus arbitration logic when the current data transfer is completed and the bus is no longer needed.
3. Output Drive Logic which contains the logic and output drivers for the memory and I/O command lines.

An external RC time constant is used with the timing logic to generate the guaranteed address set-up and hold times on the bus. The 8219 can interface directly to the 8085A CPU and the 8218 interfaces to the 8080A CPU chip and the 8257 DMA controller.

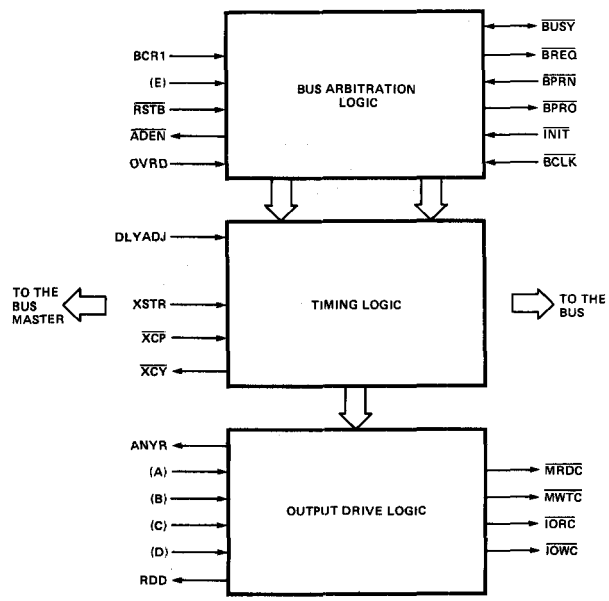
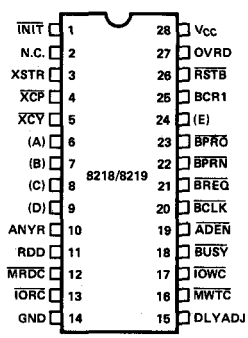


Figure 1. Block Diagram



	8218	8219
(A)	$\overline{IOWR}$	IO/$\overline{M}$
(B)	$\overline{MWTR}$	$\overline{WR}$
(C)	$\overline{IORR}$	$\overline{RD}$
(D)	$\overline{MRDR}$	$\overline{ASRQ}$
(E)	$\overline{BCR2}$	BCR2

N.C. = NO CONNECT

Figure 2. Pin Configuration

Table 1. Pin Description

Signals Interfaced Directly to the System Bus		
Symbol	**Type**	**Name and Function**
$\overline{BREQ}$	O	**Bus Request:** The Bus Request is used with a central parallel priority resolution circuit. It indicates that the device needs to access the bus for one or more data transfers. It is synchronized with the Bus Clock.
$\overline{BUSY}$	I/O	**Bus Busy:** Bus Busy indicates to all master devices on the bus that the bus is in use. It inhibits any other device from getting the bus. It is synchronized with Bus Clock.
$\overline{BCLK}$	I	**Bus Clock:** The negative edge of Bus Clock is used to synchronize the bus contention resolution circuit asynchronously to the CPU clock. It has 100ns min. period, 35%–65% duty cycle. It may be slowed, single stepped or stopped.
$\overline{BPRN}$	I	**Bus Priority In:** The Bus Priority In indicates to a device that no device of a higher priority is requesting the bus. It is synchronous with the Bus clock.
$\overline{BPRO}$	O	**Bus Priority Out:** The Bus Priority Out is used with serial priority resolution circuits. Priority may be transferred to the next lower in priority as $\overline{BPRN}$.
$\overline{INIT}$	I	**Initialize:** The Initialize resets the 8218/8219 to a known internal state.
$\overline{MRDC}$	O	**Memory Read Control:** The Memory Read Control indicates that the Master is requesting a read operation from the addressed location. It is asynchronous to the Bus Clock.
$\overline{MWTC}$	O	**Memory Write Control:** The Memory Write Control indicates that data and an address have been placed on the bus by the Master and the data is to be deposited at that location. It is asynchronous to the Bus Clock.
$\overline{IORC}$	O	**I/O Read Control:** The I/O Read Control indicates that the Master is requesting a read operation from the I/O device addressed. It is asynchronous to the Bus Clock.
$\overline{IOWC}$	O	**I/O Write Control:** The I/O Write Control indicates that Data and an I/O device address has been placed on the bus by the Master and the data is to be deposited to the I/O device. It is asynchronous to the Bus Clock.
Signals Generated or Received by the Bus Master		
BCR1/$\overline{BCR2}$	I	**Bus Control Request:** Bus Control Request 1 or Bus Control Request 2 indicate to the 8218/8219 that the Master device is making a request to control the bus. BCR2 is active low in the 8218 ($\overline{BCR2}$). BCR2 is active high in the 8219.
RSTB	I	**Request Strobe:** Request Strobe latches the status of BCR1 and BCR2 into the 8218/8219. The strobe is active low in the 8218 and negative edge triggered in the 8219.

Signals Generated or Received by the Bus Master (Continued)		
Symbol	**Type**	**Name and Function**
$\overline{ADEN}$	O	**Address and Data Enable:** Address and Data Enable indicates the Master has control of the bus. It is often used to enable Address and Data Buffers on the bus. It is synchronous with Bus Clock.
RDD	O	**Read Data:** Read Data controls the direction of the bi-directional data bus drivers. It is asynchronous to the Bus Clock. A high on RDD indicates a read mode by the master.
OVRD	I	**Override:** Override inhibits automatic deselect between transfers caused by a higher priority bus request. May be used for consecutive data transfers such as read-modify-write operations. It is asynchronous to the Bus Clock.
XSTR	I	**Transfer Start Request:** Transfer Start Request indicates to the 8218/8219 that a new data transfer cycle is requested to start. It is raised for each new word transfer in a multiple data word transfer. It is asynchronous to the Bus Clock.
$\overline{XCP}$	I	**Transfer Complete:** Transfer Complete indicates to the 8218/8219 that the data has been received by the slave device in a write cycle or transmitted by the slave and received by master in a read cycle. It is asynchronous to the Bus Clock.
$\overline{XCY}$	O	**Data Transfer:** Indicates that a data transfer is in progress. It is asynchronous to the Bus Clock.
$\overline{WR}$, $\overline{RD}$, IO/$\overline{M}$	I	**Write, Read, IO/$\overline{Memory}$:** WRITE, READ, IO/Memory are the control request inputs used by the 8085 and are internally decoded by the 8219 to produce the request signals $\overline{MRDR}$, $\overline{MWTR}$, $\overline{IORR}$, $\overline{IOWR}$. They are asynchronous to the Bus Clock. (8219 only)
$\overline{ASRQ}$	I	**Asynchronous Bus Request:** Can be used for interrupt status from the 8085. Acts like a level sensitive asynchronous bus request—no RSTB needed. It is asynchronous to the Bus Clock. (8219 only)
$\overline{MRDR}$, $\overline{MWTR}$, $\overline{IORR}$, $\overline{IOWR}$	I	**Memory Read Request, Memory Write Request, I/O Read Request, or I/O Write Request:** Indicate that address and data have been placed on the bus and the appropriate request is being made to the addressed device. Only one of these inputs should be active at any one time. They are synchronous to the Bus Clock. (8218 only)
ANYR	O	**Any Request:** Any Request is the logical OR of the active state of $\overline{MRDR}$, $\overline{MWTR}$, $\overline{IORR}$, $\overline{IOWR}$. It may be tied to XSTR when the rising edge of ANYR is used to initiate a transfer.
DLYADJ	I	**Delay Adjust:** Delay Adjust is used for connection of an external capacitor and resistor to ground to adjust the required set-up and hold time of address to control signal.

FUNCTIONAL DESCRIPTION

The 8218/8219 is a bipolar Bus Control Chip which reduces component count in the interface between a master device and the system Bus. (Master device: 8080, 8085, 8257 (DMA).)

The 8218 and 8219 serve three major functions:

1. Resolve bus contention.
2. Guarantee set-up and hold time of address/data lines to I/O and Memory read/write control signals (adjustable by external capacitor).
3. Provide sufficient drive on all bus command lines.

Bus Arbitration Logic

Bus Arbitration Logic activity begins when the Master makes a request for use of the bus on BCR1 or $\overline{BCR2}$. The request is strobed in by $\overline{RSTB}$. Following the next two falling edges of the bus clock (BCLK) the 8218/8219 outputs a bus request ($\overline{BREQ}$) and forces Bus Priority Out inactive (BPRO). See Figures 1a and 1b.

$\overline{BREQ}$ is used for requesting the bus when priority is decided by a parallel priority resolver circuit.

$\overline{BPRO}$ is used to allow lower priority devices to gain the bus when a serial priority resolving structure is used. $\overline{BPRO}$ would go to $\overline{BPRN}$ of the next lower priority Master.

When priority is granted to the Master (a low on $\overline{BPRN}$ and a high on $\overline{BUSY}$) the Master outputs a $\overline{BUSY}$ signal on the next falling edge of $\overline{BCLK}$. The $\overline{BUSY}$ signal locks the master onto the bus and prohibits the enable of any other masters onto the bus.

At the same time $\overline{BUSY}$ goes active, Address and Data Enable ($\overline{ADEN}$) goes active signifying that the Master has control of the bus. $\overline{ADEN}$ is often used to enable the bus drivers.

The Bus will be released only if the master loses priority; is not in the middle of a transfer, and Override is not active or, if the Master stops requesting the bus, is not in the middle of a data transfer, and Override is not active. $\overline{ADEN}$ then goes inactive.

Provision has been made in the 8218 to allow bus-synchronous requests. This mode is activated when BCR1, $\overline{BCR2}$ and $\overline{RSTB}$ are all low. This action asynchronously sets the synchronization flip flop (FF2) in Figure 3a.

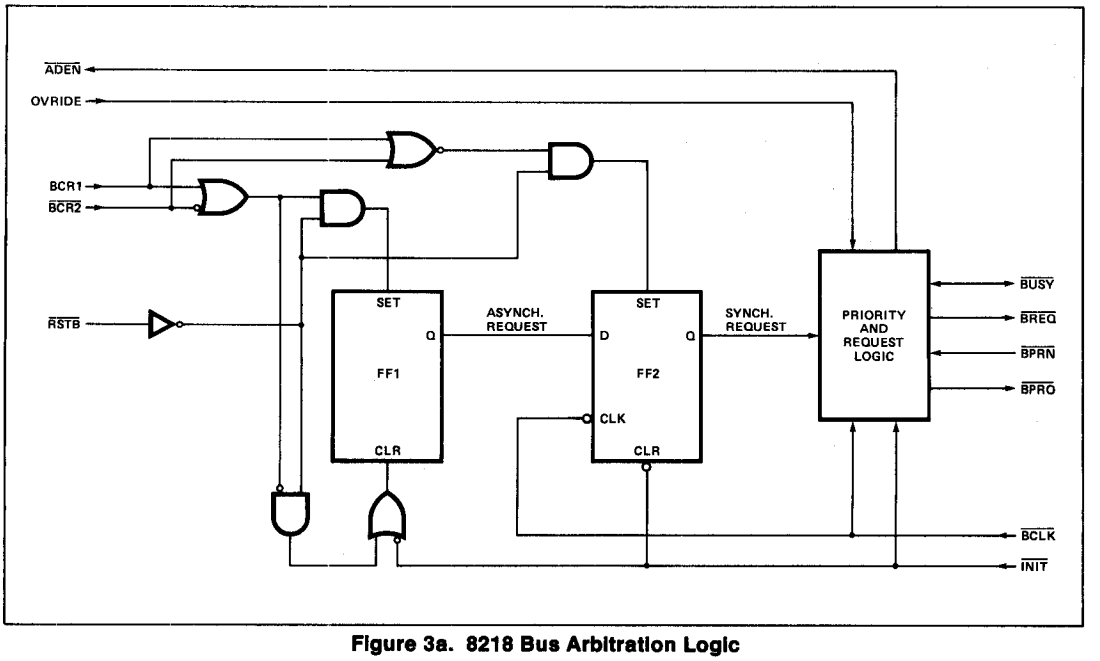


Figure 3a. 8218 Bus Arbitration Logic

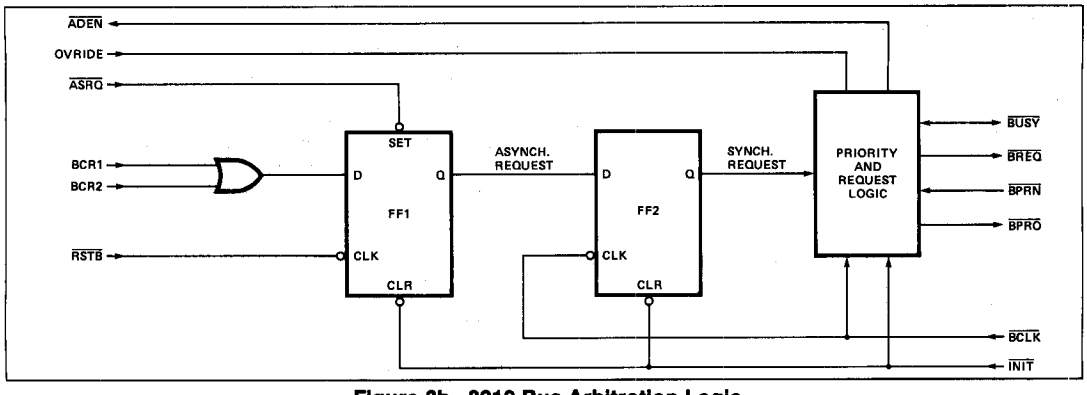


Figure 3b. 8219 Bus Arbitration Logic

Timing Logic

Timing Logic activity begins with the rising edge of XSTR (Transfer Start Request) or with $\overline{ADEN}$ going active, whichever occurs second. This action causes $\overline{XCY}$ (Transfer Cycle) to go active. 50-200ns later (depending on resistance and capacitance at DLYADJ) the appropriate Control Outputs will go active if the control input is active.

XSTR can be raised after the command goes active in the current transfer cycle so that a new transfer can be initiated immediately after the current transfer is complete.

A negative going edge on $\overline{XCP}$ (Transfer Complete) will cause the Control Outputs ($\overline{MRDC}$, etc.) to go inactive. 50-200ns later (depending on capacitance at DLYADJ) $\overline{XCY}$ will go inactive indicating the transfer cycle is completed.

Additional logic within the 8218/8219 guarantees that if a transfer cycle is started ($\overline{XCY}$ is active), but the bus is not requested ($\overline{BREQ}$ is inactive) and there is no command request input (ANYR is output low), then the transfer cycle will be cleared. This allows the bus to be released in applications where advanced bus requests are generated but the processor enters a HALT mode.

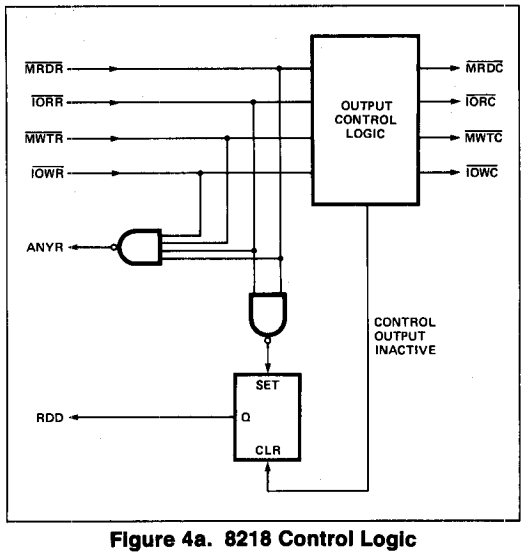


Figure 4a. 8218 Control Logic

Control Logic

The control outputs are generated in the 8219 by decoding the 8085 system control outputs (i.e., RD, WR, IO/M) or in the 8218 by directly buffering the control inputs to the control outputs for use in an 8080 or DMA system (see Figures 4a and 4b). The control outputs may be held high (inactive) by the Timing Logic. Also the control outputs are enabled when the Master gains control of the bus and disabled when control is relinquished.

The Control Logic also has two other outputs, ANYR (Any Request) and RDD (Read Data). ANYR goes high (active) if any control requests (IOWR, etc.) are active. RDD controls the direction of the Masters Bi-directional Data Bus Drivers. The Bus Driver will always be in the Write mode (RDD = Low) except from the start of a Read Control Request to 25 to 70ns after $\overline{XCP}$ is activated.

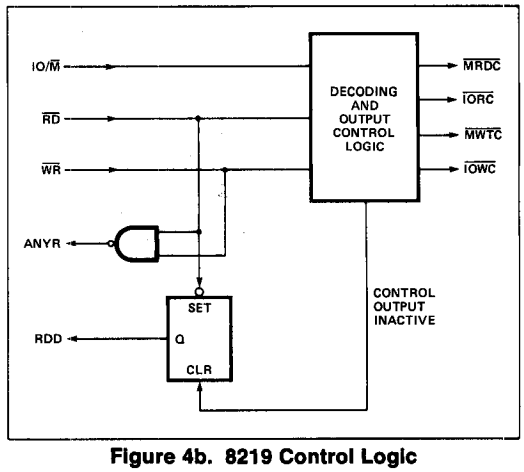


Figure 4b. 8219 Control Logic

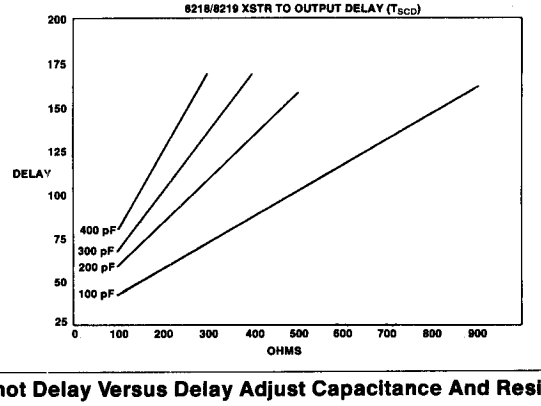
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage (V_{CC}) ..... -0.5V to +7V
Input Voltage ..... -1.0V to V_{CC} + 0.25V
Output Current 100mA

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_C	Input Clamp Voltage			-1.0	V	V_{CC} = 4.75V, I_C = -5mA
I_F	Input Load Current $\overline{MRDR}/\overline{INTA}/\overline{MWTR}/\overline{WR}$ $\overline{IORR}/\overline{RD}$, IOWR/IO/$\overline{M}$			-0.5	mA	V_{CC} = 5.25V V_F = 0.45V
	Other			-0.5	mA	
I_R	Input Leakage Current			100	μA	V_{CC} = 5.25 V_R = 5.25
V_{TH}	Input Threshold Voltage	0.8		2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		200	240	mA	V_{CC} = 5.25V
V_{OL}	Output Low Voltage					V_{CC} = 4.75
	$\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$			0.45	V	I_{OL} = 32mA
	$\overline{BREQ}$, $\overline{BUSY}$			0.45	V	I_{OL} = 20mA
	$\overline{XCY}$, $\overline{RDD}$, $\overline{ADEN}$			0.45	V	I_{OL} = 16mA
	$\overline{BPRO}$, ANYR			0.45	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage					V_{CC} = 4.75V
	$\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$ $\overline{BUSY}$ O.C.	2.4				I_{OH} = -2mA
	All Other Outputs	2.4				I_{OH} = -400μA
I_{OS}	Short Circuit Output Current	-10		-90	mA	V_{CC} = 5.25V, V_O = 0V
$I_{O\ (OFF)}$	Tri-State Output Current			-100	μA	V_{CC} = 5.25V, V_O = 0.45V
				+100	μA	V_{CC} = 5.25V, V_O = 5.25V
C_{IN}	Input Capacitance Except Busy		10	20	pF	
C_{IO}	Input Capacitance Busy		25	35	pF	

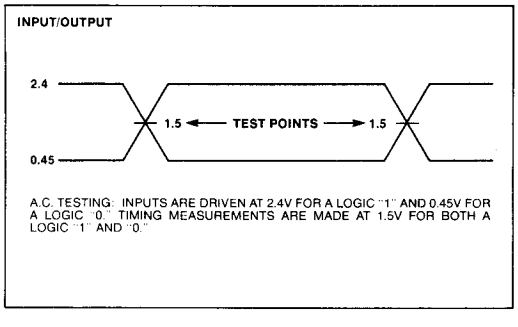


One Shot Delay Versus Delay Adjust Capacitance And Resistance

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

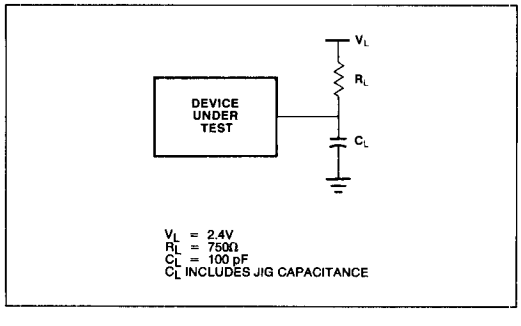
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{BCY}	Bus Clock Cycle Time	100			ns	35% to 65% Duty Cycle
t_{PW}	Bus Clock Pulse Width	35		0.65 t_{BCY}	ns	
t_{RQS}	$\overline{RSTB}$ to $\overline{BCLK}$ Set-Up Time	25			ns	
t_{CSS}	BCR_1 and $\overline{BCR_2}$ to $\overline{RSTB}$ Set-Up Time	15			ns	
t_{CSH}	BCR_1 and $\overline{BCR_2}$ to $\overline{RSTB}$ Hold Time	15			ns	
t_{RQD}	$\overline{BCLK}$ to $\overline{BREQ}$ Delay			35	ns	
t_{PRNS}	$\overline{BPRN}$ to $\overline{BCLK}$ Set-Up Time	23			ns	
t_{BNO}	$\overline{BRPN}$ to $\overline{BPRO}$ Delay			30	ns	
t_{BYD}	$\overline{BCLK}$ to $\overline{BUSY}$ Delay			55	ns	
t_{CAD}	$\overline{MRDR}$, $\overline{MWTR}$, $\overline{IORR}$, $\overline{IOWR}$ to ANYR Delay			30	ns	
t_{SXD}	XSTR to $\overline{XCY}$ Delay			40	ns	
t_{SCD}	XSTR to $\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$ Delay	50		200	ns	Adjustable by External R/C
t_{XSW}	XSTR Pulse Width	30			ns	
t_{XCD}	$\overline{XCP}$ to $\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$ Delay			50	ns	
t_{XCW}	$\overline{XCP}$ Pulse Width	35			ns	
t_{CCD}	$\overline{XCP}$ to $\overline{XCY}$ Delay	50		200	ns	Adjustable by External R/C
t_{CMD}	$\overline{MRDR}$, $\overline{MWTR}$, $\overline{IORR}$, $\overline{IOWR}$ to $\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$			35	ns	
t_{CRD}	$\overline{MRDR}$, $\overline{MWTR}$, $\overline{IORR}$, $\overline{IOWR}$ to RDD Delay			25	ns	
t_{RW}	$\overline{RSTB}$ Min. Neg. Pulse Width	30			ns	
t_{CPD}	$\overline{BCLK}$ to $\overline{BPRO}$ Delay			40	ns	
t_{XRD}	$\overline{XCP}$ to $\overline{RDD}$ Delay	25		70	ns	

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0."

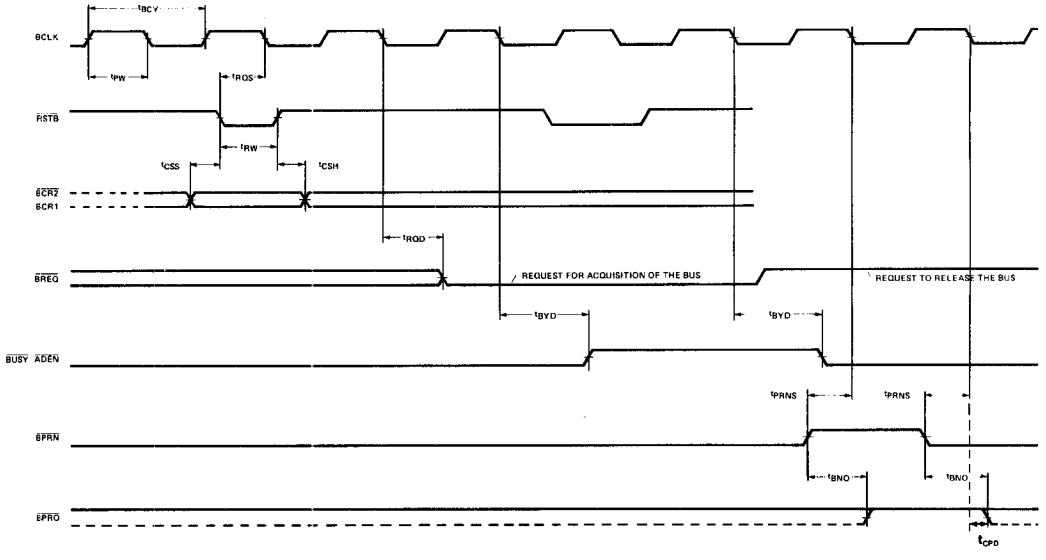
A.C. TESTING LOAD CIRCUIT



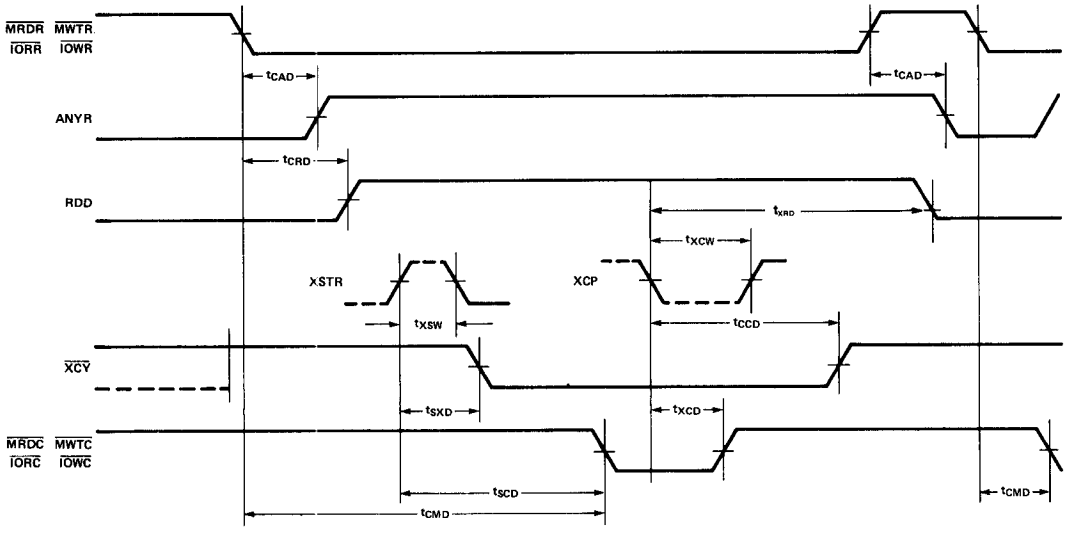
V_L = 2.4V
R_L = 750Ω
C_L = 100 pF
C_L INCLUDES JIG CAPACITANCE

WAVEFORMS

SYNCHRONOUS BUS TIMING (System Bus Previously Not In Use)

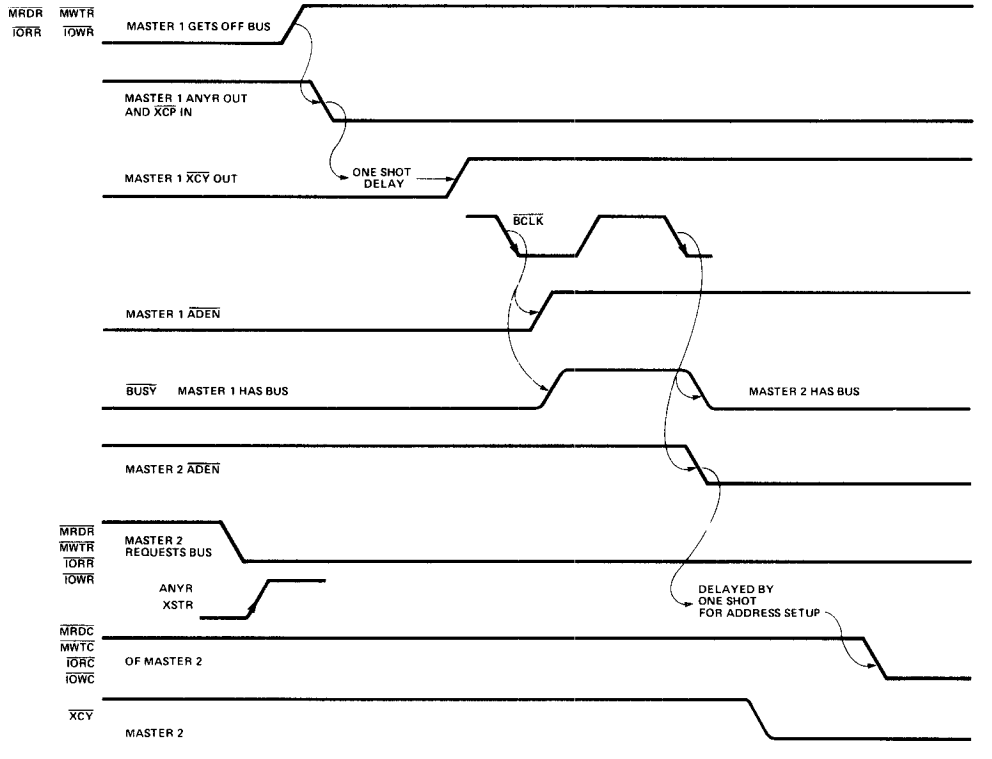


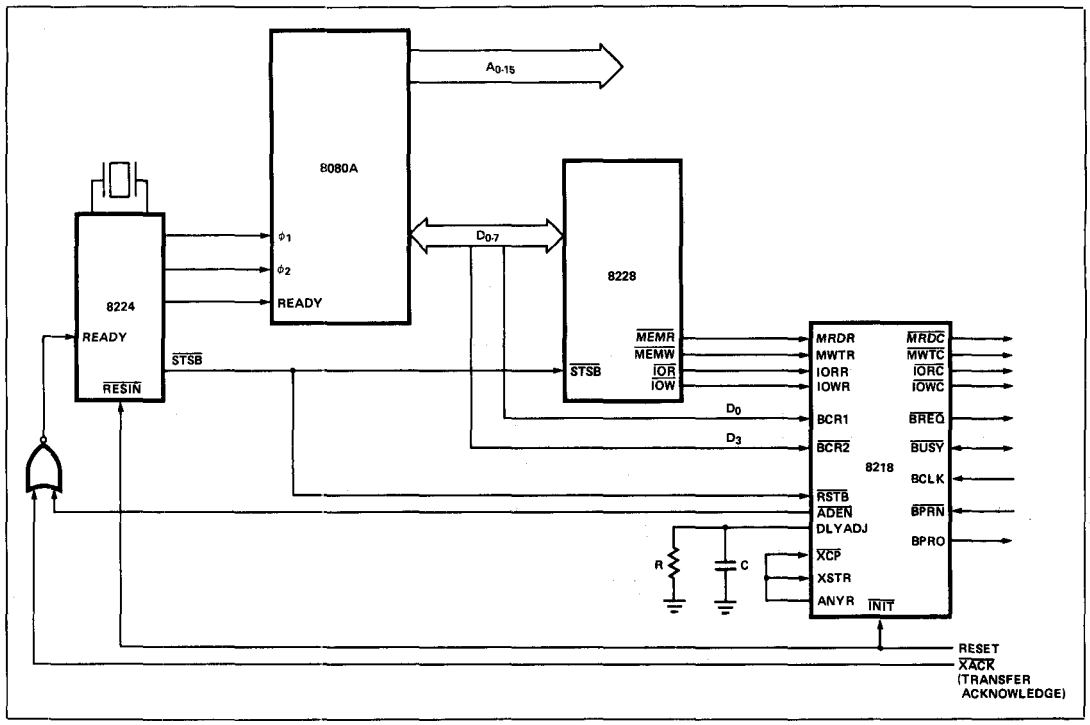
CONTROL CYCLE (System Bus Previously Not In Use)



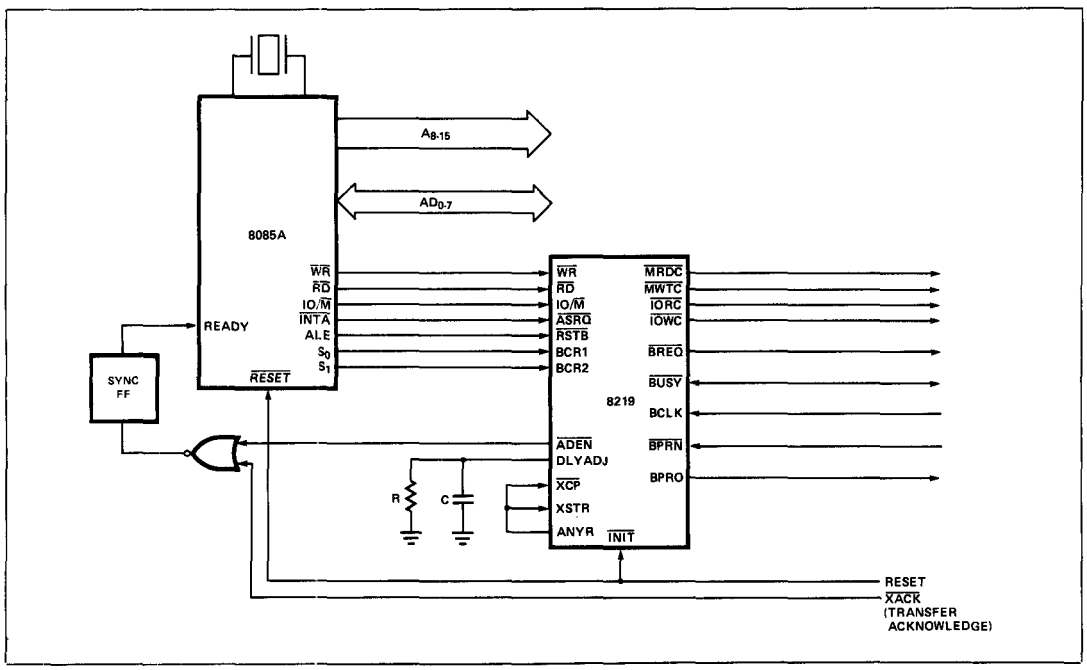
WAVEFORMS (Continued)

BUS CONTROL EXCHANGE (Master No. 1 Leaving Bus And Master No. 2 Getting On Bus)

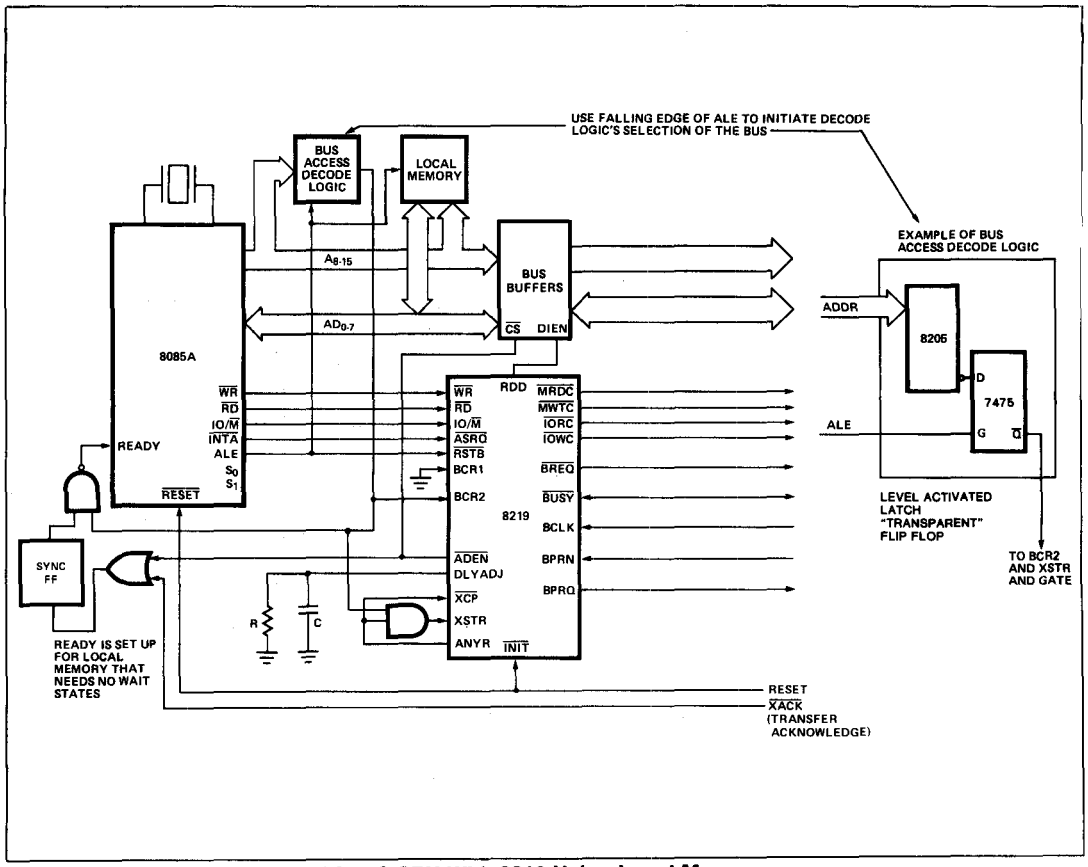




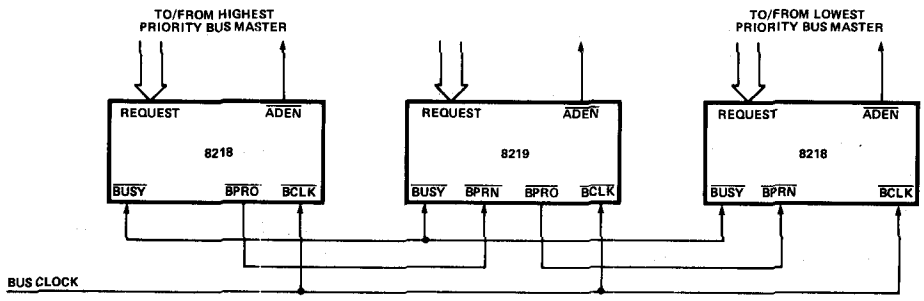
MCS-80® CPU With 8218



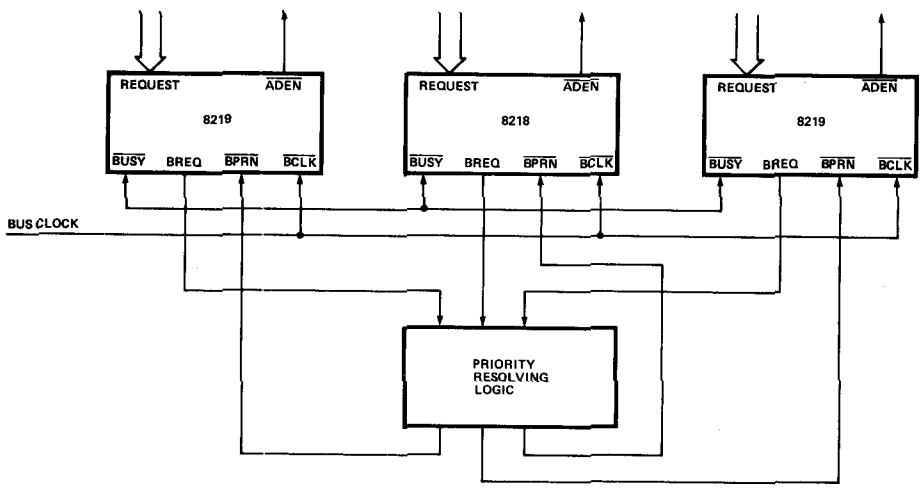
MCS-85® CPU With 8219



MCS-85® CPU With 8219 Using Local Memory



"DAISY CHAIN" CONFIGURATION



PARALLEL REQUEST CONFIGURATION

Two Methods of Connecting Multiple 8218/8219's To Resolve Bus Contention Among Multiple Masters